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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,135	10/31/2003	Ulf Tohsche	W&B-INF-1980	3466

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,135	TOHSCHE, ULF	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 11-01-04. Applicant' arguments with respect to references of Kojima, Oklobdzija and Japanese reference have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remain rejected under these references. The rejection changes slightly for clarification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kojima et al. (US Pat. 6,445,217).

Regarding claims 1 and 16, figure 6 and 8 of Kojima show a flip-flop, comprising:

a clock input (C), a data input (D), a non-inverted output (Q), an inverted output (Q/);

a data acceptance unit (128, 129, 630, 632) having a first second switching element (630, 632);

a storage unit (134-137) having first and second inverter circuits (134, 135) connected in a feedback loop to provide feedback between said first and second inverter circuits;

Depending upon the data and the clock signal, the switching elements (630, 632) apply a "predetermined programming potential " and a ground potential or zero potential or no potential to the inputs of the storage unit (134-137).

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Oklobdzija et al. (US Pat. 6,232,810).

Regarding claims 1 and 16, figure 6A and 7 of Oklobdzija show a flip-flop, comprising:

a clock input (Clk), a data input (D), a non-inverted output (Q), an inverted output (Q/);

a data acceptance unit (101, 34, 36) having a first second switching element (T1, 34 and T5, 36);

a storage unit (32) having first and second inverter circuits (82, 84) connected in a feedback loop to provide feedback between said first and second inverter circuits;

Depending upon the data and the clock signal, the switching elements apply a "predetermined programming potential" and a ground potential to the inputs of the storage unit (32).

Regarding claims 2-4, figures 6A and 7 show that the first switching element (T1, 32) is activated when the clock is high and the data is at high level and is inhibited when the clock is at low level.

Regarding claims 5 and 6, the "a first partially clocked inverter" comprising transistors (T2-T4) that convert a high level data input to a low level signal (S/). The first switching element (T1, 34) receives low-level signal (S/) when the clock signal is high and the data is high. Signal (S/) becomes low when the clock is high and the data is low.

Regarding claims 7-9, figures 6A and 7 show that the second switching element (T5, 36) is activated when the clock is high and the data is at high level and is inhibited when the clock is at low level.

Regarding claim 10, figure 7 shows that when the clock changes from a low level to a high level, data (D) is transferred to storage unit in complementary form (S/, R/) and to be stored.

Claims 1-10 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated Japanese reference No. 10093397.

Regarding claims 1 and 16, the reference shows a flip-flop, comprising:

a clock input (CLK), a data input (D), a non-inverted output (Q), an inverted output (QN);

a data acceptance unit (A, B, 4, 5, 6, 7) having a first second switching element (4, 5 and 6, 7);

a storage unit (8, 9) having first and second inverter circuits connected in a feedback loop to provide feedback between said first and second inverter circuits;

Depending upon the data and the clock signal, the switching elements apply a "predetermined programming potential " and a high impedance or "no potential" to the inputs of the storage unit.

Regarding claim 2, when the data signal (D) and the clock signal (CKL) are at high level, the first switching unit (6, 7) in activated and when the data signal or the clock signal is at low level, the first switching unit is inhibited.

Regarding claims 3 and 4, when the clock signal (CKL) are at high level and the data signal (D) is at low level, the second switching unit (4, 5) in activated and when the clock signal is at low level and the data signal is at high level, the first switching unit is inhibited.

Regarding claims 5 and 6, the first partially clock inverter (B) has an output coupled to the first switching element (6, 7). When the clock signal is at low level (second level) and the data is at low level (second level), a low level signal is applied to first switching element (6, 7).

Regarding claims 7 and 8, the second partially clocked inverter (A) is coupled to the second switching element (4, 5). The second partially clocked inverter (A) applies an inverted data signal (DN) to the second switching element (4, 5) when the clock signal is low. The first partially clocked inverter (B) applies a non-inverted data signal (D) to the first switching element (6, 7) when the clock signal is low.

Regarding claim 9 and 10, the circuit of the Japanese reference clearly shows the transferring of data depending upon the level of the data and the clock signals. When the clock signal changes from a low level to a high level, data (D) is transferred to storage unit in complementary form (D and DN) and to be stored in the storage unit.

Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Collier et al. (US 2003/0006812 A1).

Regarding claims 1-4, figure 1a of Collier shows a flip-flop comprising: a clock input (CLK), a data input (D, DB), a non inverted output (Q), an inverted output (QB), a data acceptance unit (N5, N6), a storage unit comprising inverters (P1, N1), (P2, N2) having first and second input; and

said data acceptance unit allocating, dependent upon the data signal (D, DB) present and the clock signal (CLK) present, a predetermined programming potential either to said first input or to said second input and to apply "no potential" to the respective other input of said first and second inverter circuits, said first switching element (N5) of said data acceptance unit applying said predetermined programming potential to said first input dependent upon the clock signal and the data signal, and said second switching element (N6) of said data acceptance unit applying said predetermined programming potential to said second input dependent upon the clock signal and the data signal. The first switch is activated when the clock signal and the data signal are high.

Claims 1-4 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomokazu Kouno (SHO 60[1985]-224319).

Regarding claims 1-4, figure 11 of Kouno shows a flip-flop comprising: a clock input (CL1), a data input (DIN, /DIN), a non inverted output (M), an inverted output (/M), a data acceptance unit (7, 8), a storage unit (6) comprising inverters having first and second input; and

said data acceptance unit allocating, dependent upon the data signal (DIN, /DIN) present and the clock signal (CL1) present, a predetermined programming potential either to said first input or to said second input and to apply "no potential" to the respective other input of said first and second inverter circuits, said first switching element of said data acceptance unit applying said predetermined programming potential to said first input dependent upon the clock signal (low) and the data signal, and said second switching element of said data acceptance unit applying said predetermined programming potential to said second input dependent upon the clock signal and the data signal. The first switch is activated when the clock signal and the data signal are high.

Regarding claim 11, the activation input is the gate of transistor (15) receiving an activation signal (/RES). When the activation signal (/RES) is low, transistor (15) in turned off and the flip-flop is deactivated, and the storage unit remains stored independently of the clock signal and the data signal present.

Response to Arguments

In the Remarks page 28, the Applicant argues that " the Kojima reference fails to....and **no potential** to the other input" lines 4-7. These arguments are not persuasive. A "potential" is a voltage with **respect to a reference voltage** (ground or **zero volt**) applied to a node of a circuit. When the voltage at that node is **zero volt potential or at ground level potential**, there is **no voltage** or **no potential** applied to that node. In the claim the Applicant recited only "no potential" thus, the Kojima reference does teach a "**no potential**" as recited in claims 1 and 16. The Japanese reference shows that when data (D) is high, transistors (4) turned off and transistor (6) is turned on. With a high level of the clock, transistor (6) and (7) are turned on and a low input is applied to the storage unit and the other terminal of the storage unit is connected to a high impedance or "no potential" because transistor (4) is turned off.

In page 29, again the Applicant argues that " At no time does one of the logic blocks 34, 36, apply a potential to one input of the storage block 32 while the other logic block 34, 36 applies no potential (i.e. a high impedance, not recited in the claim), so that the voltage level at the respective input is not affected by the data acceptance unit". Figure 7 and 6A of Oklobdzija shows that Oklobdzija show that, in the **active region**, signals IS and IR are always in **opposite polarities**. Transistors 62 and 64 are **all p-channel transistors**. Thus, one of them is turned on and the transistor that is turned off thus, providing **high impedance** (no potential) to the inputs of the storage unit (32). Because of the feedback property of inverters (82, 84) or because of the feedback loop in the storage unit (32), one of the outputs (Q, /Q) of the storage unit (34) is high and the other is low or vice versa (not affected by the data acceptance unit). Therefore, Oklobdzija fully teaches all the limitations of claims 1 and 16.

Conclusion

The claims have serious 112, first and second paragraph problems. The Applicant is requested to amend the claims so that one skilled in the art can understand the meaning of the claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
01-10-05

TUAN T. LAM
PRIMARY EXAMINER